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Sheet	1	of	2	Attorney Docket Number	351891.01700
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### Complete if known

Application Number	09/340,580
Filing Date	June 28, 1999
First Named Inventor	Chung-Wah, Norris IP
Group Art Unit	2128
Examiner Name	Pham, Thai Q.

### U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.*	U.S. Patent Document		Name of Patentee or Applicant Of Cited Document	Date of Publication of Cited Document MM- DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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### U.S. PATENT PUBLICATIONS

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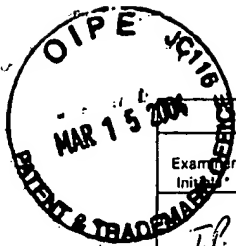
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### OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T*
T.P.	A1	Pitro Zafiropulo, Colin H. West, Harry Rudin, D.D. Cowan, and Daniel Brand (April 1980) "Towards Analyzing and Synthesizing Protocols," <i>IEEE Transactions on Communications</i> , 28 (4)	
T.P.	A2	A. Bouajjani, S. Bensalem, S. Graf, C. Loiseaux, and J. Sifakis (1993) "Property Preserving Abstractions for the Verification of Concurrent Systems," <i>Formal Methods in System Design</i> , 6(1):11-44	
T.P.	A3	J.R. Burch, E.M. Clarke, K.L. McMillan, D.L. Dill, and L.J. Hwang (1990) "Symbolic Model Checking: 10 <sup>20</sup> States and Beyond," <i>5<sup>th</sup> IEEE Symposium on Logic in Computer Science</i>	
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T.P.	A5	U. Stern and D.L. Dill (1995) "Improved Probabilistic Verification by Hash Compaction," <i>Advanced Research Working Conference on Correct Hardware Design and Verification Methods</i>	
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T.P.	A7	Elaine J. Weyuker and Bingchiang Jeng (July 1991) "Analyzing Partition Testing Strategies," <i>IEEE Transactions on Software Engineering</i> , Vol. 17, No. 7. July 1991.	
T.P.	A8	Daniel Lenoski, James Laudon, Kourosh Gharachorloo, Wolf-Dietrich Weber, Anoop Gupta, John Hennessy, Mark Horowitz, and Monica Lam (1992) "The Stanford DASH Multiprocessor," <i>Computer</i> , 25(3)	
T.P.	A9	A. Chandra, V. Iyengar, D. Jameson, R. Jawalekar, I Nair, B. Rosen, M. Mullen, J. Yoon, R. Armoni, D. Geist, and Y. Wolfsthal (1995) "AVPGEN - A Test Generator for Architecture Verification," <i>IEEE Transactions on VLSI Systems</i> , Vol. 3, No. 2	
T.P.	A10	"Spec-Based Verification," <i>Verisity Design, Inc.</i> , (June 1998)	

**OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T*
T.P.	A11	S. Bose and A.L. Fisher (1989), "Verifying Pipelined Hardware Using Symbolic Logic Simulation," <i>International Conference on Computer Design: VLSI in Computers and Processors</i> .	
T.P.	A12	C. Han Yang and David L. Dill (1998), "Validation With Guided Search of the State Space," <i>35th Design Automation Conference</i>	

Examiner Signature	<i>Maughan</i>	Date Considered	1/14/05
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